FIG.1 PRIOR ART

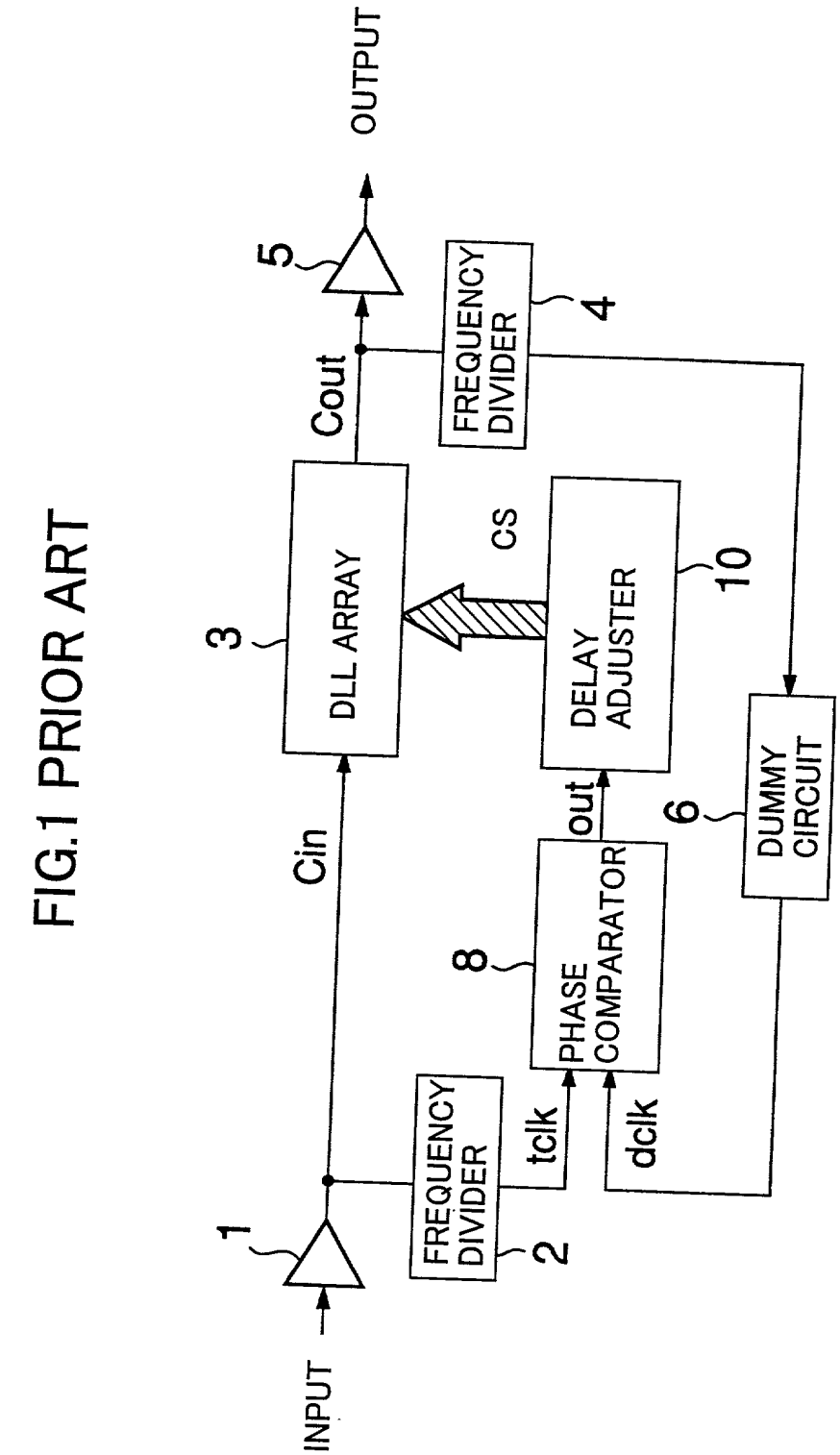


FIG.2 PRIOT ART

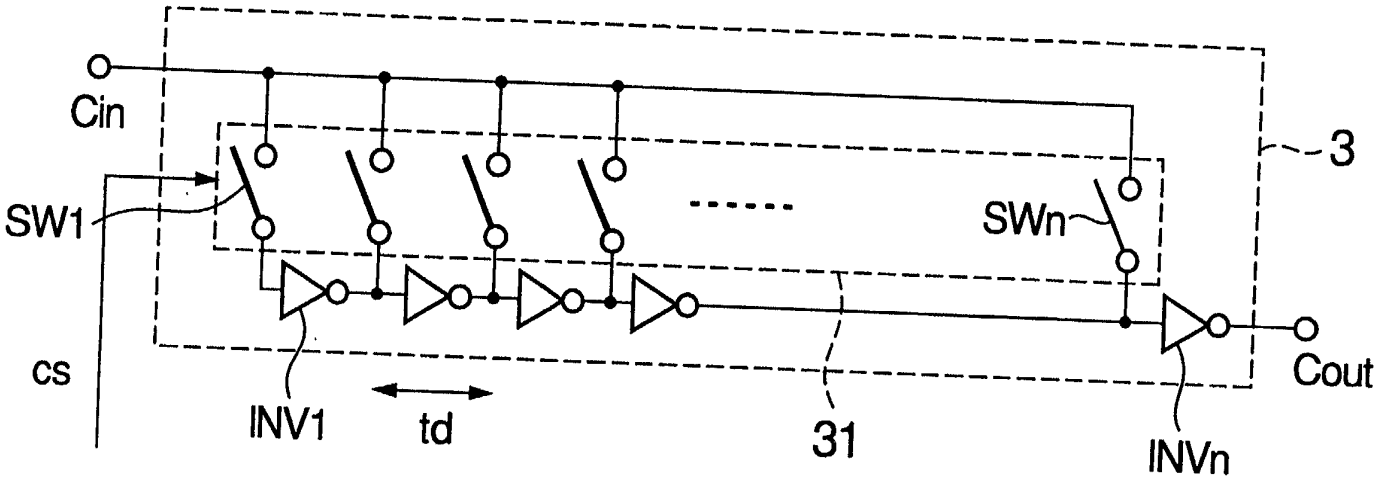


FIG.3
PRIOR
ART

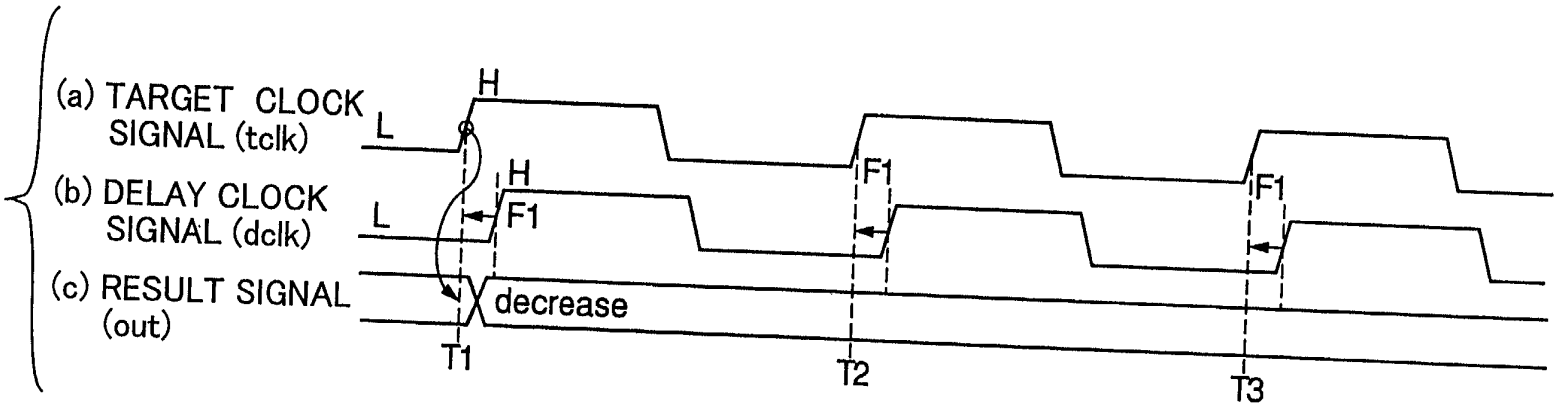


FIG.4
PRIOR
ART

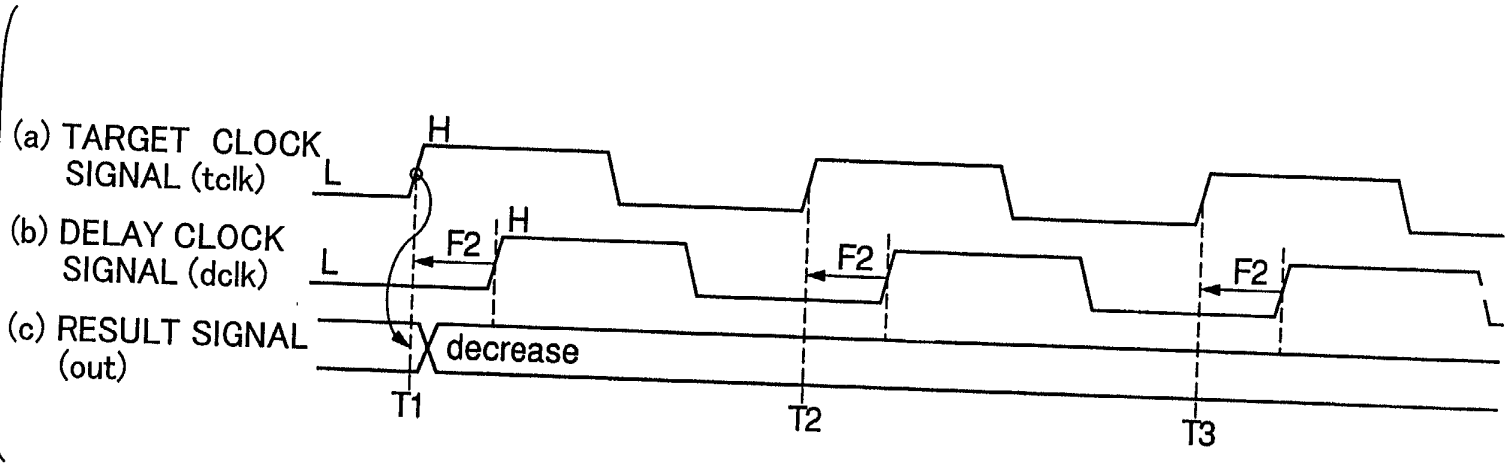


FIG.5
PRIOR
ART

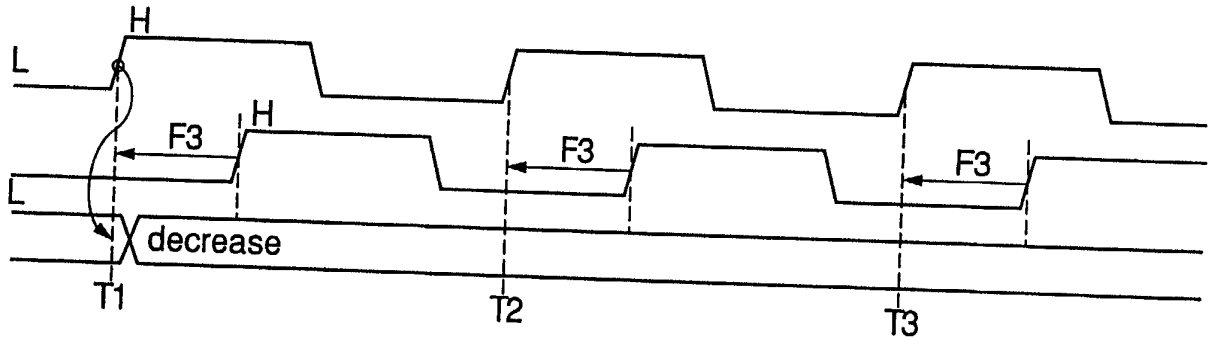


FIG.6
PRIOR
ART

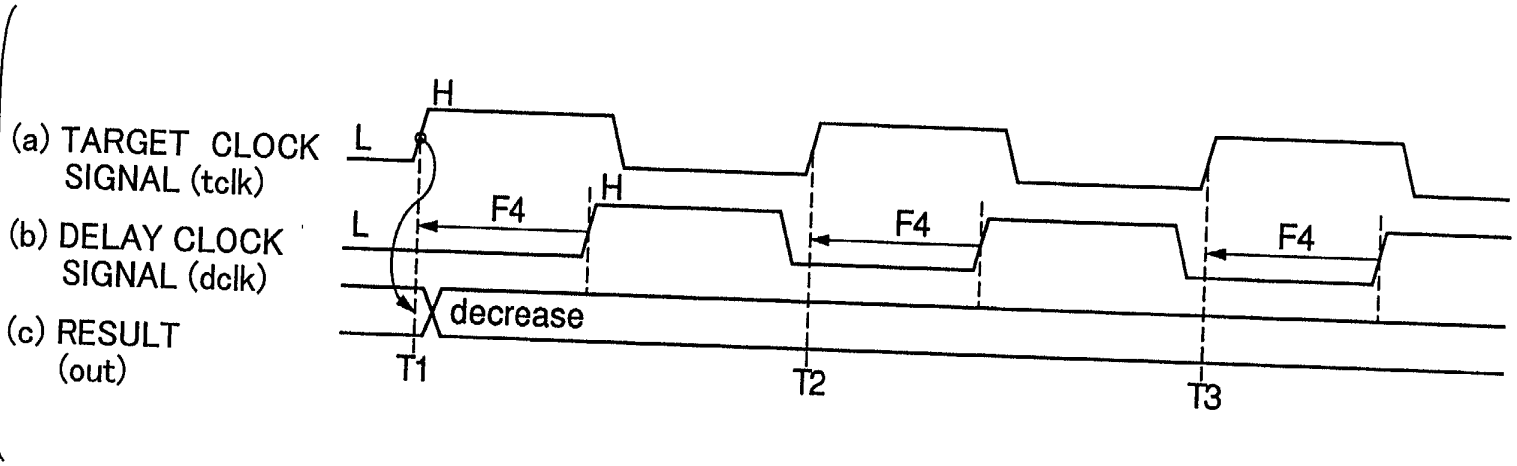


FIG.7
PRIOR
ART

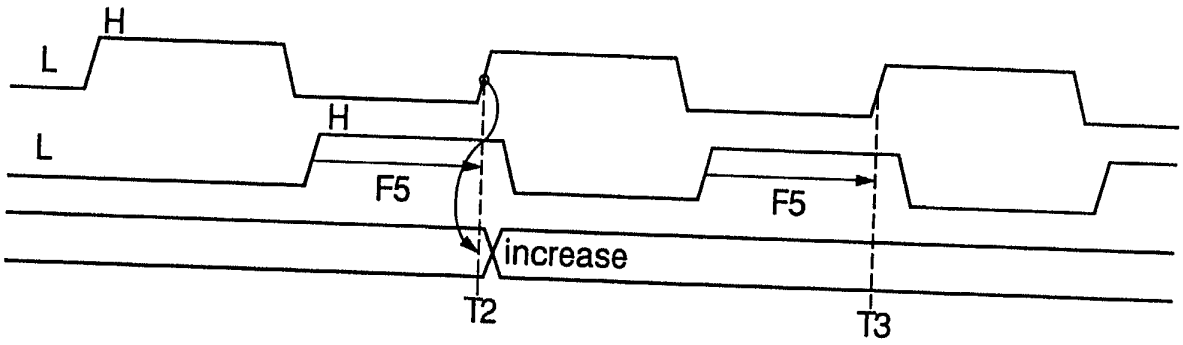


FIG. 8 PRIOR ART

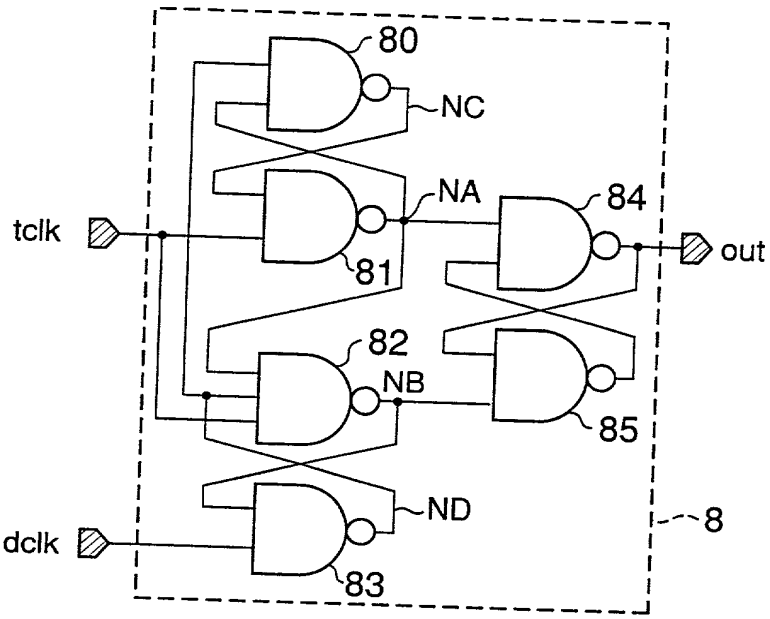


FIG. 9
PRIOR
ART

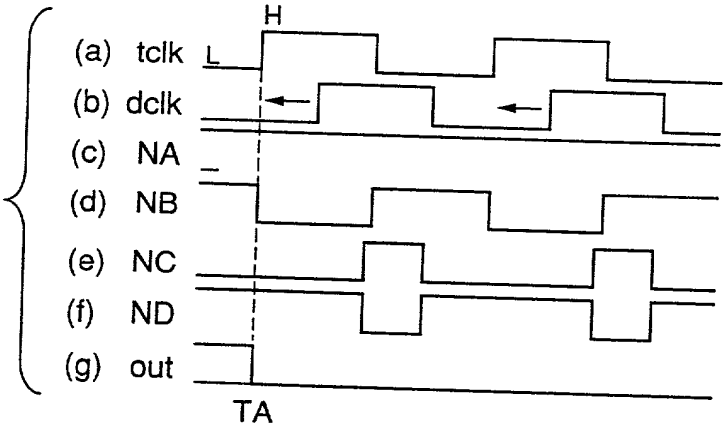


FIG. 10
PRIOR
ART

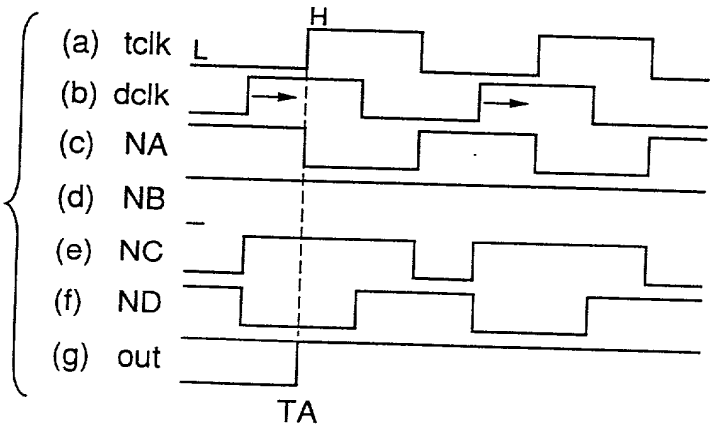


FIG.11

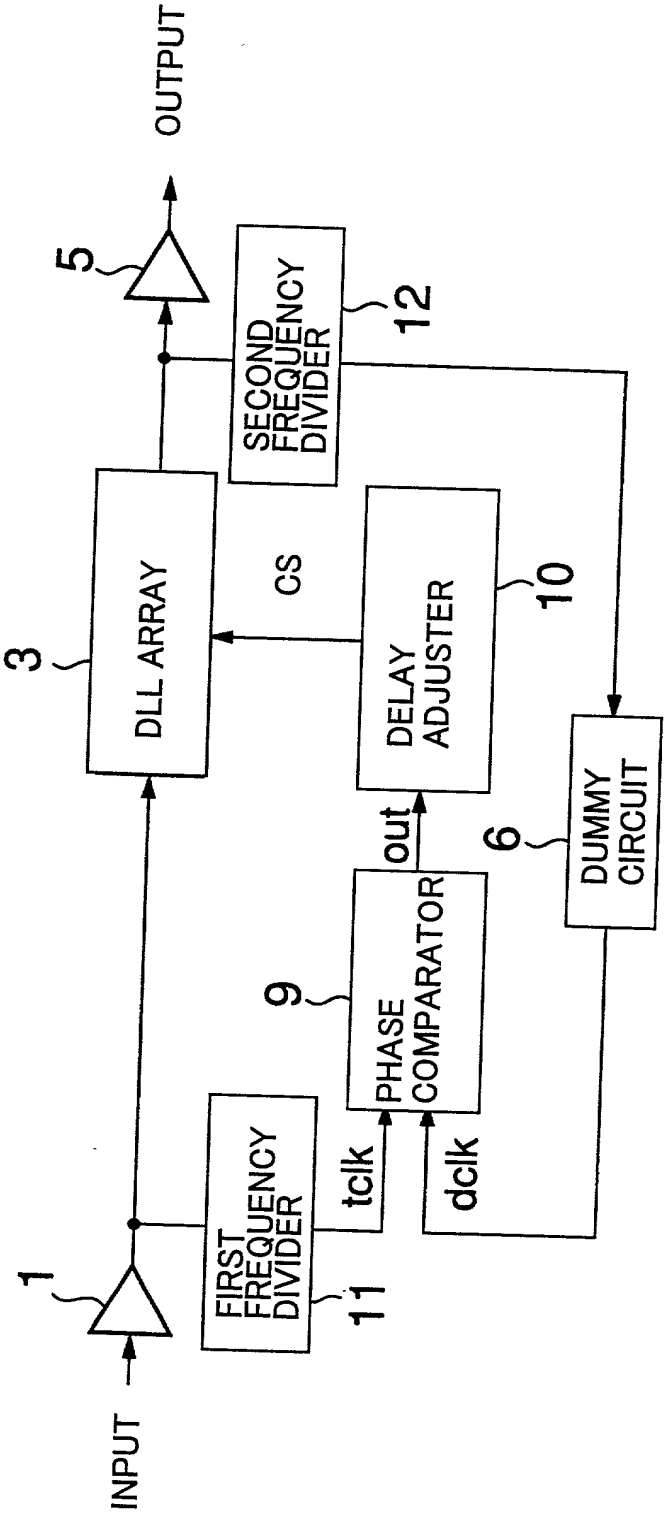

INPUT
1
FIRST FREQUENCY DIVIDER
11
tclk
dclk
9
PHASE COMPARATOR
out
6
DUMMY CIRCUIT
3
DLL ARRAY
CS
DELAY ADJUSTER
10
SECOND FREQUENCY DIVIDER
12
5
OUTPUT

FIG.12

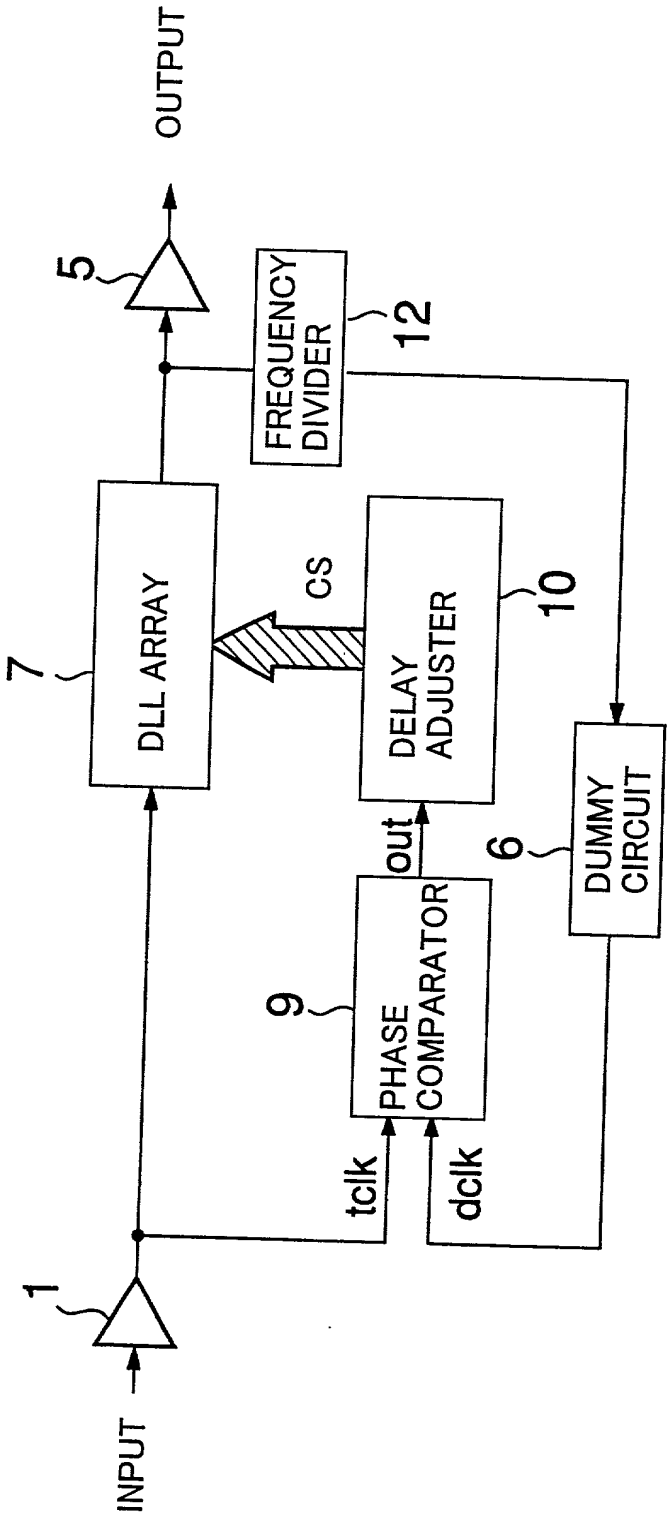

INPUT
1
tclk
dclk
9
PHASE COMPARATOR
out
6
DUMMY CIRCUIT
7
DLL ARRAY
CS
DELAY ADJUSTER
10
FREQUENCY DIVIDER
12
5
OUTPUT

FIG.13

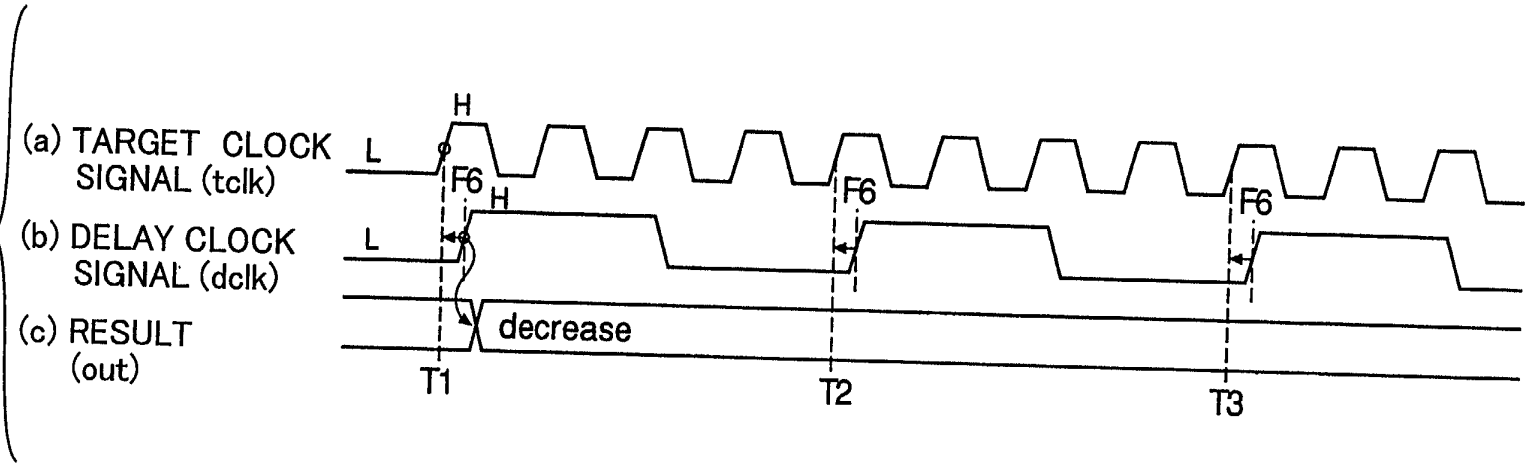


FIG.14

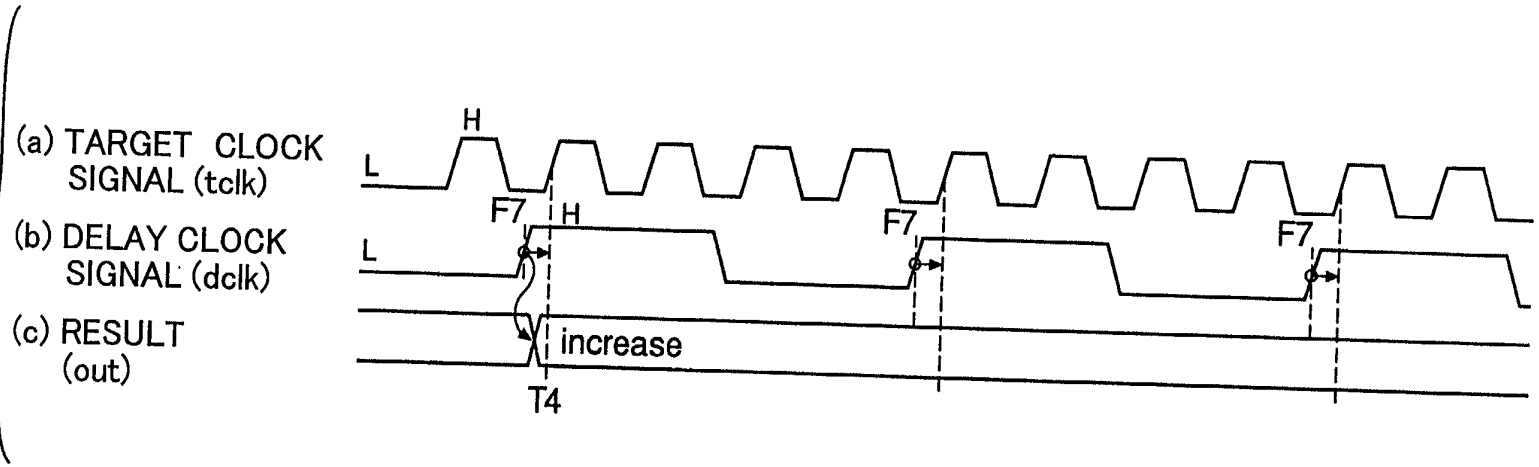

(a) TARGET CLOCK SIGNAL (tclk)
(b) DELAY CLOCK SIGNAL (dclk)
(c) RESULT (out)
H
L
F7
H
L
F7
F7
increase
T4

FIG.15

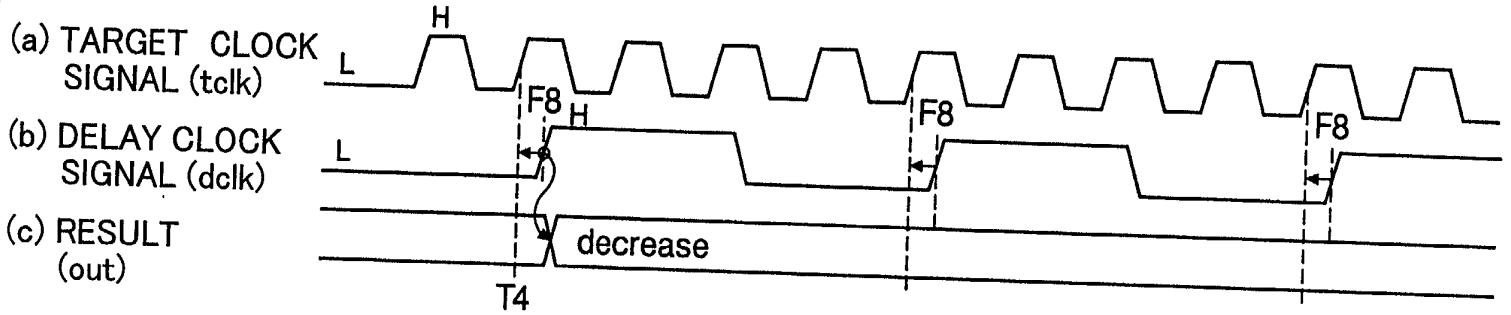


FIG.16

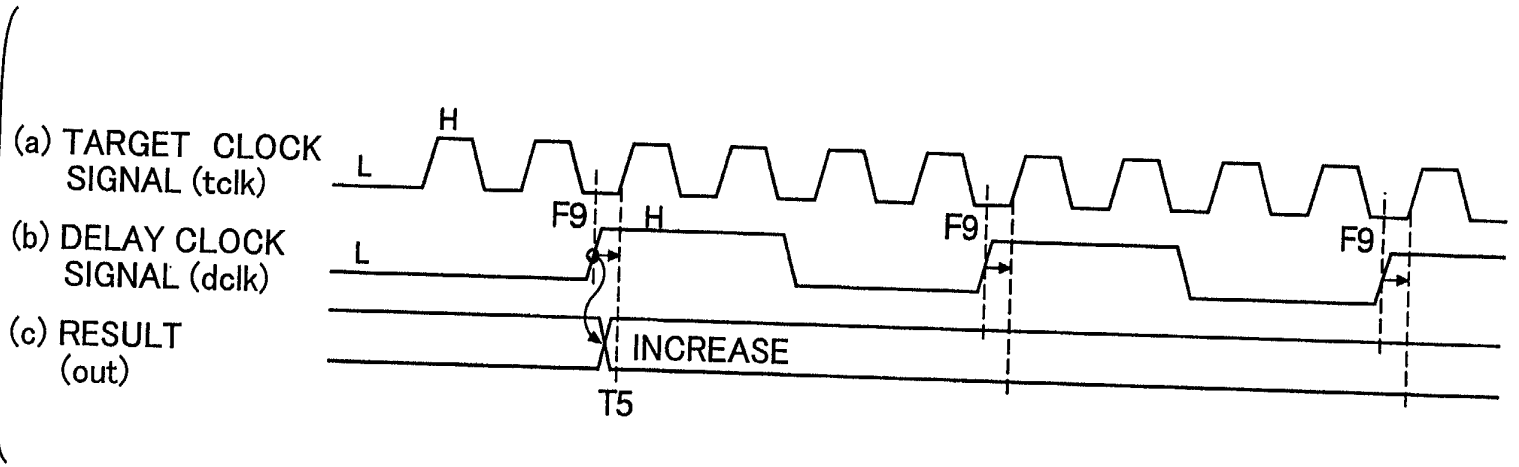

(a) TARGET CLOCK SIGNAL (tclk)
(b) DELAY CLOCK SIGNAL (dclk)
(c) RESULT (out)
H
L
F9
H
L
F9
F9
INCREASE
T5

FIG.17

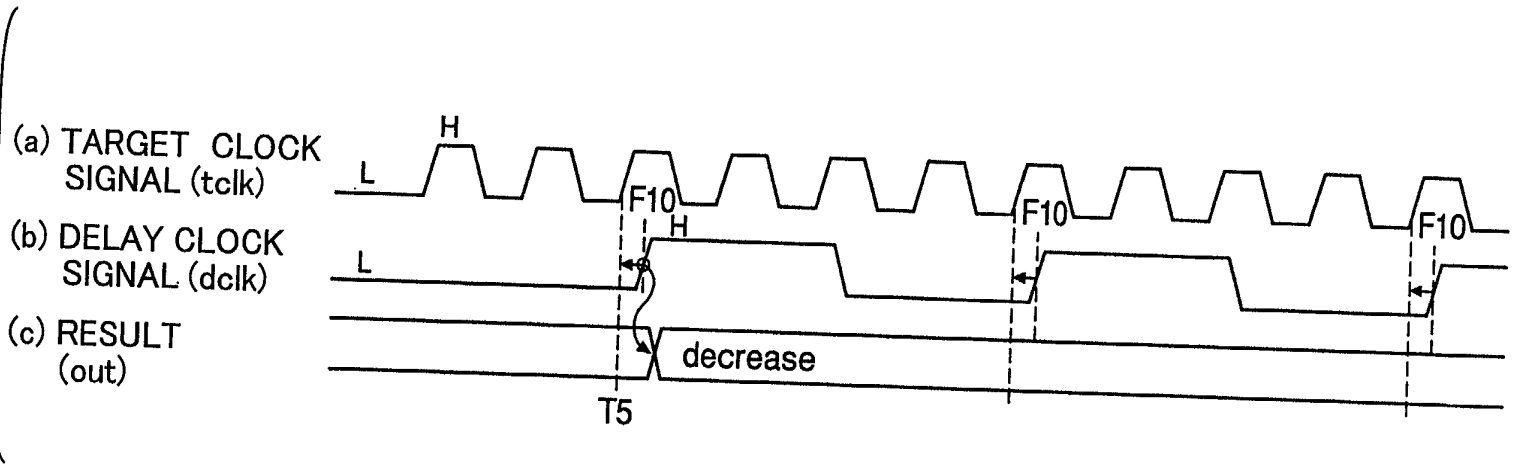

(a) TARGET CLOCK SIGNAL (tclk)
(b) DELAY CLOCK SIGNAL (dclk)
(c) RESULT (out)
H
L
F10
H
L
F10
F10
decrease
T5

FIG. 18

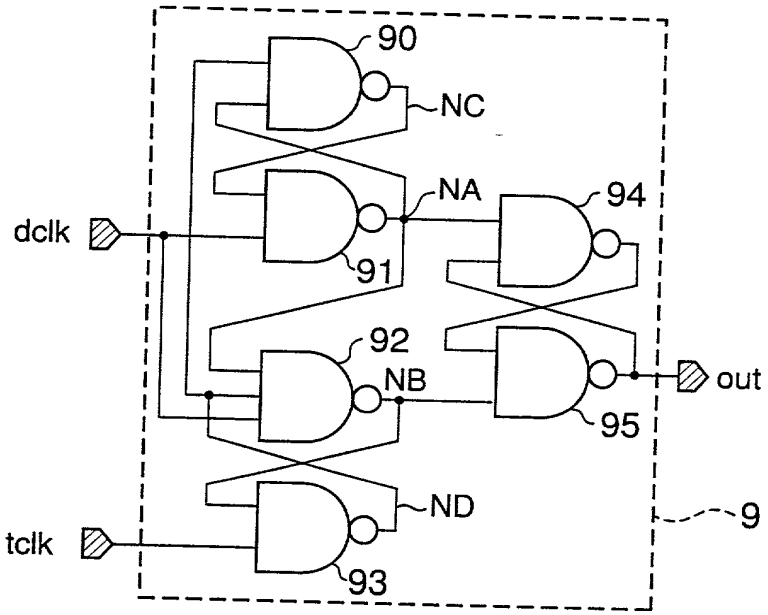


FIG. 19

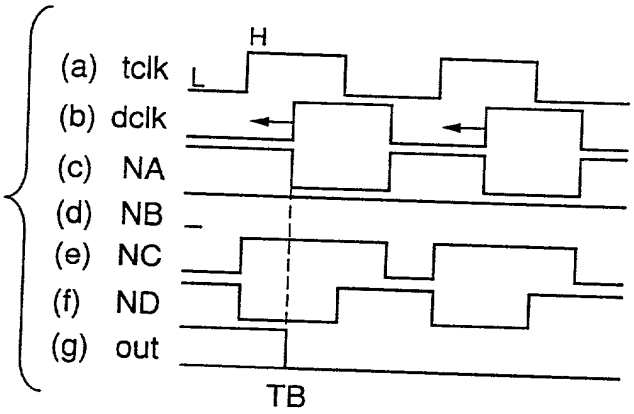
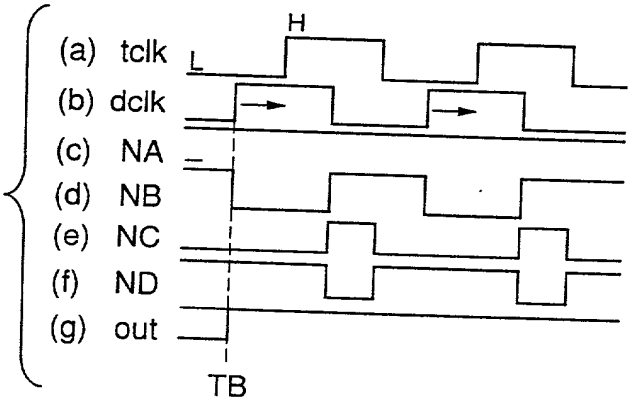

H
L
(a) tclk
(b) dclk
(c) NA
(d) NB
(e) NC
(f) ND
(g) out
TB

FIG. 20


H
L
(a) tclk
(b) dclk
(c) NA
(d) NB
(e) NC
(f) ND
(g) out
TB